MAPPING SYSTEM AND METHOD FOR INSTRUCTION SET PROCESSING

ABSTRACT OF THE DISCLOSURE

A method, cache controller, and computer processor provide a parallel mapping system whereby a plurality of mappers processes several inputs simultaneously. The plurality of mappers are disposed in a pipelined processor upstream from a multiplexor. Mapping, tag comparison, and selection by the multiplexor all occur in a single pipeline stage. Data does not wait idly to be selected by the multiplexor. Instead, each instruction of a first instruction set is read in parallel into a corresponding one of the plurality of mappers. This parallel mapping system implementation reduces processor cycle time and results in improved processor efficiency.